TEMIC

Siliconix

VP2410L

P-Channel Enhancement-Mode MOS Transistor

Product Summary

Part Number	$V_{(BR)DSS}$ Min (V)	$r_{DS(on)}$ Max (Ω)	$V_{GS(th)}$ (V)	I_D (A)
VP2410L	−240	10 @ V_{GS} = −4.5 V	−0.8 to −2.5	−0.18

Features

- High-Side Switching
- Secondary Breakdown Free: −255 V
- Low On-Resistance: 8 Ω
- Low-Power/Voltage Driven
- Excellent Thermal Stability

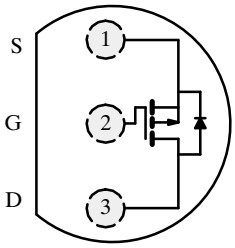
Benefits

- Ease in Driving Switches
- Full-Voltage Operation
- Low Offset Voltage
- Easily Driven Without Buffer
- No High-Temperature "Run-Away"

Applications

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Power Supply, Converters
- Motor Control
- Switches

TO-226AA
(TO-92)



Top View

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V_{DS}	−240	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	−0.18	A
	T_A = 100°C		−0.11	
Pulsed Drain Current		I_{DM}	−0.72	
Power Dissipation	T_A = 25°C	P_D	0.8	W
	T_A = 100°C		0.32	
Maximum Junction-to-Ambient		R_{thJA}	156	°C/W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Notes
a. Pulse width limited by maximum junction temperature.

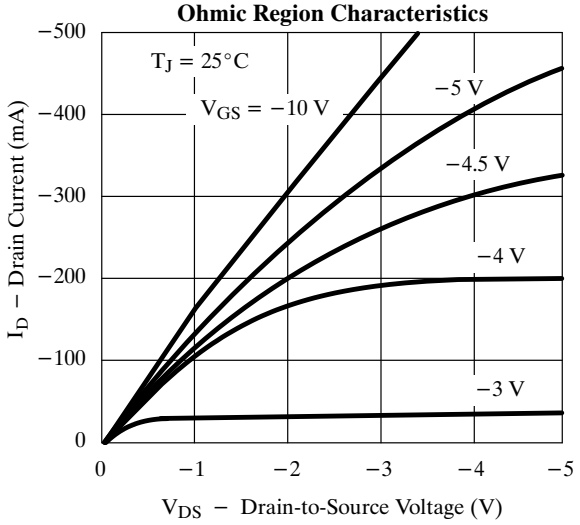
Specifications[a]

Parameter	Symbol	Test Conditions	Limits Min	Limits Typ[b]	Limits Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −5 µA	−240	−255		V
		V_{GS} = 0 V, I_D = −10 µA		−255		
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −1 mA		−2.1		
		V_{DS} = V_{GS}, I_D = −2.5 mA	−0.8	−2.2	−2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
		T_J = 125°C			±50	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −180 V, V_{GS} = 0 V			−1	µA
		T_J = 125°C			−100	
On-State Drain Current[c]	$I_{D(on)}$	V_{DS} = −10 V, V_{GS} = −4.5 V	−150	−300		mA
Drain-Source On-Resistance[c]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −0.1 A		6		Ω
		V_{GS} = −4.5 V, I_D = −0.1 A		8	10	
		T_J = 125°C		14.5	20	
Forward Transconductance[c]	g_{fs}	V_{DS} = −10 V, I_D = −0.1 A	125	175		mS
Common Source Output Conductance[c]	g_{os}	V_{DS} = −10 V, I_D = −0.05 A		0.125		
Dynamic						
Input Capacitance	C_{iss}	V_{DS} = −25 V, V_{GS} = 0 V f = 1 MHz		65	95	pF
Output Capacitance	C_{oss}			25	30	
Reverse Transfer Capacitance	C_{rss}			12	15	
Switching[d]						
Turn-On Time	t_{ON}	V_{DD} = −25 V, R_L = 250 Ω I_D ≅ −0.1 A, V_{GEN} = −10 V R_G = 25 Ω		25		ns
	$t_{d(on)}$			7	15	
	t_r			18	30	
Turn-Off Time	t_{OFF}			90		
	$t_{d(off)}$			45	70	
	t_f			45	60	

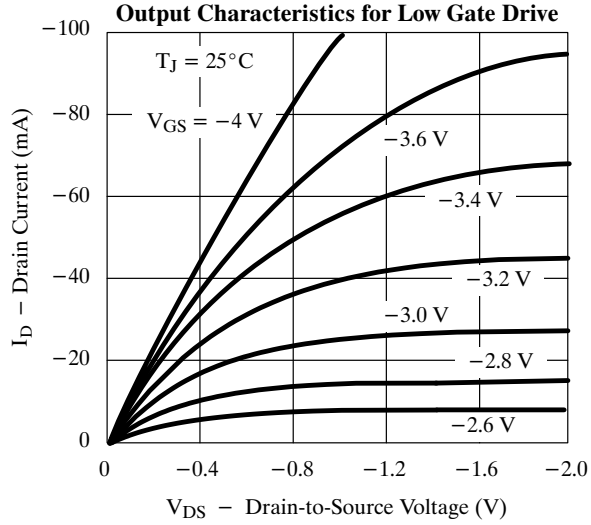
Notes
a. T_A = 25°C unless otherwise noted. VPDV24
b. For DESIGN AID ONLY, not subject to production testing.
c. Pulse test: PW ≤ 300 µs duty cycle ≤ 2%.
d. Switching time is essentially independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

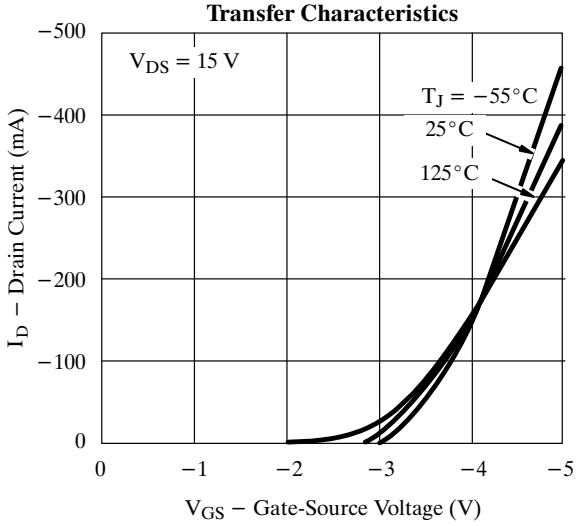
Ohmic Region Characteristics



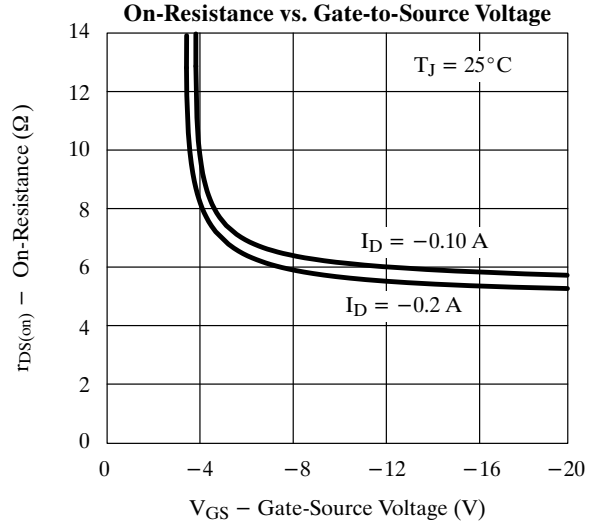
Output Characteristics for Low Gate Drive



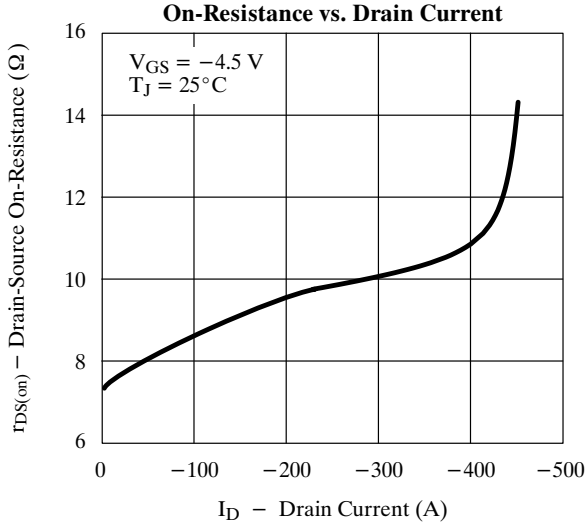
Transfer Characteristics



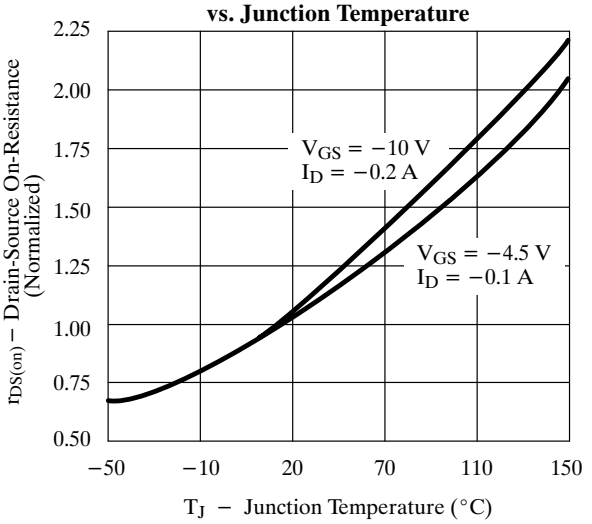
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Drain Current

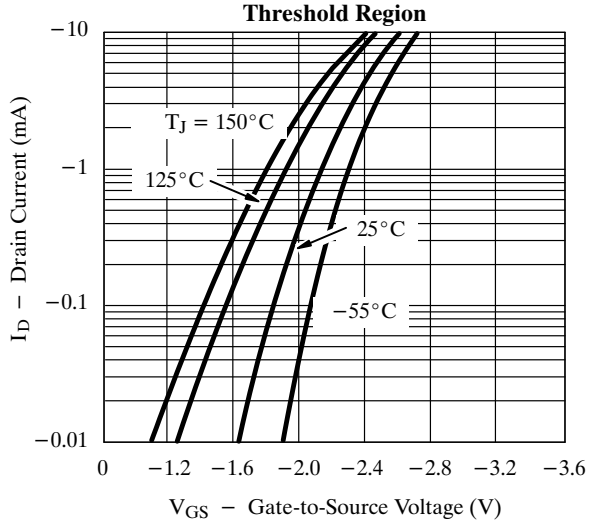


Normalized On-Resistance vs. Junction Temperature

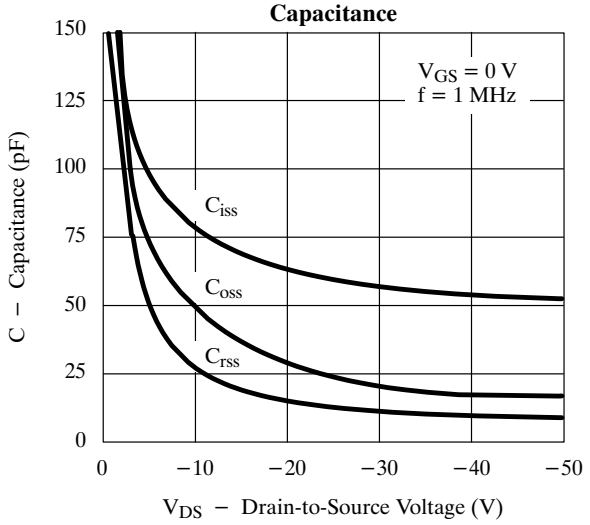


Typical Characteristics (25°C Unless Otherwise Noted) (Cont'd)

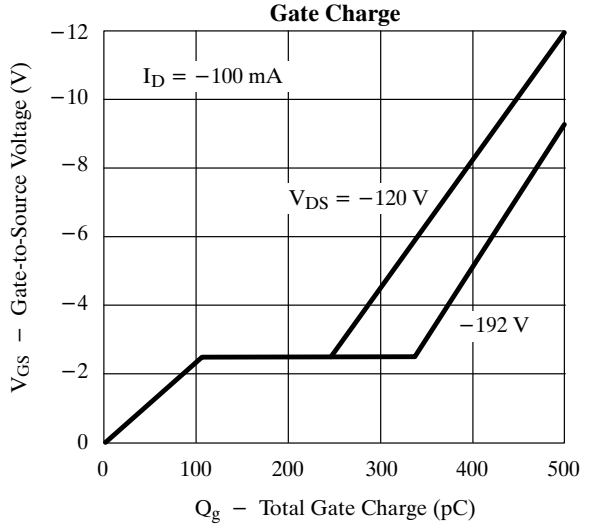
Threshold Region



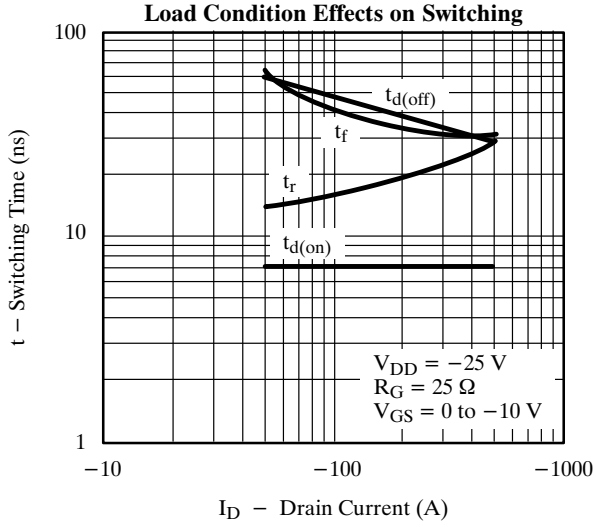
Capacitance



Gate Charge



Load Condition Effects on Switching



Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-226AA)